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JAMES J MURPHY
5400 RENAISSANCE TOWER
1201 ELM STREET
DALLAS, TX 752702199

EXAMINER	
WOOD, WILLIAM H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/435,070	Applicant(s) SINHAROY, BALARAM	
	Examiner William H. Wood	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10 and 21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10 and 21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 August 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 10 and 21-40 have been examined.

Specification

1. The disclosure is objected to because of the following informalities: Applicant amended the paragraph beginning at line 3 on page 13 by replacing the number 402 with 401 as indicated on page 20 of the amendment submitted on 28 August 2002. This new element number does not seem to appear in Figures 4 or 3A. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-2, 24-26, 28, 29, 31-36 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257.

In regard to claim 21, Patt disclosed the limitations:

i) *a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address* (page 253, bracket 4)

ii) a fetch-based history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register (page 253, bracket 5)

iii) each entry of the fetch-based branch history table operable for containing bits representing a prediction value for a plurality of branches in a fetch group (page 253, bracket 5; a fetch group here being nothing more that what is fetched)

iv) a selector table comprising a plurality of entries each for storing a plurality of selection bits and accessed by a pointer generated from selected bits from said branch address and bits from said history register (page 252, bracket 1 and page 255, section 4.1)

v) each said selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from said fetch-based history table (page 255, bracket A and Figure 2)

In regard to claim 22, Patt disclosed the limitations:

i) circuitry for updating said bimodal and fetch-based branch history tables (page 253, section 3 and 3.1)

ii) set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time (the tables are set to at least two values in order to predict at least taken and not-taken)

iii) *set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time* (the tables are set to at least two values in order to predict at least taken and not-taken)

In regard to claim 24, Patt disclosed the limitations:

i) *circuitry for updating said selector table* (page 252, bracket 3)

ii) *update a corresponding bit in a selected entry in said selector table with a first value when a bimodal prediction value from said bimodal branch history table correctly represents a corresponding branch resolution* (page 252, bracket 3)

iii) *update a corresponding bit in a selected entry in said selector table with a second value when a fetch-based prediction value from said fetch-based branch history table correctly represents the corresponding branch resolution* (page 252, bracket 3)

In regard to claim 25, Patt disclosed the limitation *wherein the plurality of selection bits are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table* (page 255, section 4.1)

In regard to claim 26, Patt disclosed the limitations:

i) *wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when corresponding values from said bimodal and fetch-based branch history tables both correctly represent a corresponding branch resolution* (page 252, bracket 3)

ii) *and wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when neither values from said bimodal and fetch-based branch history tables correctly represents a corresponding branch resolution* (page 252, bracket 3)

In regard to claim 28, Patt disclosed the limitations:

i) *a first branch history table comprising a plurality of bimodally accessed entries, each entry for storing a first set of branch prediction bits* (page 253, bracket 4)

ii) *a second branch history table comprising a plurality of fetch-based accessed entries each entry for storing a second set of branch prediction bits* (page 253, bracket 5)

iii) *a selector for selecting, in response to a plurality of selection control bits, a set of prediction bits from a selected one of said sets of bits accessed from said first and second branch history tables* (page 255, section 4.1 and page 252 bracket 1)

iv) *a selector table comprising a plurality of entries, each entry for storing a plurality of selection bits wherein the selection control bits are set as a function of a performance history of corresponding first and second sets of branch prediction*

bits stored in said first and second branch history tables (page 255, section 4.1 and page 252 bracket 1)

In regard to claim 29, Patt disclosed the limitation *wherein said entries of said selector table are accessed using fetch-based accessing* (page 255, section 4.1 and in particular brackets 6 and 7).

In regard to claim 31, Patt disclosed the limitation *wherein said first and second branch history tables and said selector table form a portion of a branch execution unit* (page 252, Abstract).

In regard to claim 32, Patt disclosed the limitation *wherein said branch execution unit forms a part of a microprocessor* (page 252, Abstract).

In regard to claim 33, Patt disclosed the limitation *further comprising memory coupled to said microprocessor* (the branch selection predictors and tables themselves form "memory").

In regard to claim 34, Patt disclosed the limitations:

i) *a method of performing branch predictions in a processing system including a bimodal branch history table, a fetch-based branch history table and a selector table* (page 252, bracket 1; page 253, brackets 4 and 5, page 252, Abstract)

ii) *accessing the bimodal branch history table to retrieve a first set of branch prediction bits* (page 255, section 4.1)

iii) *accessing the fetch-based branch history table to retrieve a set of second branch prediction bits* (page 255, section 4.1)

iv) *selecting between the first and second sets of branch prediction bits in response to corresponding bits retrieved from the selector table* (page 255, section 4.1)

v) *wherein a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits is not less than a number of instructions in a fetch group* (page 255, section 4.1; a fetch group in Patt might be defined as no larger than 1)

vi) *updating the selector table as a function of actual branch resolution* (page 252, bracket 3)

In regard to claim 35, Patt disclosed the limitations:

i) *determining if at least one of the first set of branch prediction bits correctly predicts the corresponding branch resolution outcome* (page 252, bracket 3)

ii) *updating the corresponding entry in the selector table to a first logic value when the at least one of the first set of prediction bits correctly represents the branch resolution outcome* (page 252, bracket 3)

iii) *determining if at least one of the second set of branch prediction bits correctly predicts the branch resolution outcome* (page 252, bracket 3)

iv) *updating the corresponding entry in the selector table to a second logic value when the at least one of the second set of branch prediction bits correctly represents the branch resolution outcome* (page 252, bracket 3)

In regard to claim 36, Patt disclosed the limitations:

i) *determining if at least one bit of both the first and second sets of branch history bits correctly predict the branch resolution outcome* (page 252, bracket 3)

ii) *maintaining the current value of the corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome* (page 252, bracket 3)

iii) *determining if at least one bit of both the first and second sets of branch prediction bits incorrectly predict the branch resolution outcome* (page 252, bracket 3)

iv) *maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch history bits incorrectly predict the branch history outcome* (page 252, bracket 3)

In regard to claim 38, Patt disclosed the limitation *wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from*

at least some bits of a branching instruction and bits retrieved from a history register (page 253, bracket 5).

Claim Rejections - 35 USC § 103

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257 in view of Hennessy et al. Computer Architecture: A Quantitative Approach, Morgan Kaufmann Publishers, Inc.; pp. 269.

In regard to claim 10, Patt disclosed the following limitations:

i) *a first branch history table comprising a plurality of bimodally accessed entries for storing a first set of branch prediction bits* (page 253, bracket 4)

ii) *a second branch history table comprising a plurality of fetch-based accessed entries for storing a second set of branch prediction bits* (page 253, bracket 5)

iii) a selector for selecting from a selected one of said sets of bits accessed from said first and second branch history tables (page 255, section 4.1)

iv) a selector table comprising a plurality of entries for storing said a set of selector bits as a function of a performance history of said first and second sets of branch prediction bits stored in said first and second branch history tables (page 255, section 4.1)

Patt did not explicitly state *a selection bit*. Official Notice is taken that it was known at the time of invention to use one single bit is all that is required for selecting. It would

have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's selection system such that only one of the bits is ultimately used to select. This implementation would have been obvious because one of ordinary skill in the art would be motivated to simplify the circuitry and thus become more efficient.

Patt did not explicitly state *wherein said each said entry in said tables comprises a 1-bit counter.* Hennessy demonstrated that it was known at the time of invention to use n-bit counters (page 269). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's counters as 1-bit counters as suggested by Hennessy's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implement a 1-bit counter as the simplest type of counter in order to reduce the circuit design for cost or space constraints.

5. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257, as applied to claim 28 above, and in view of Hennessy et al. Computer Architecture: A Quantitative Approach, Morgan Kaufmann Publishers, Inc.; pp. 269.

In regard to claim 30, Patt did not explicitly state *wherein said each said entry in said tables comprises a 1-bit counter.* Hennessy demonstrated that it was known at the time of invention to use n-bit counters (page 269). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's counters as 1-bit

counters as suggested by Hennessy's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implement a 1-bit counter as the simplest type of counter in order to reduce the circuit design for cost or space constraints.

6. Claims 23, 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257, as applied to claims 21 and 38 above, respectively, and in view of McFarling, "Combining Branch Predictors".

In regard to claim 23, Patt did not explicitly state *wherein said history register comprises shift register and said branch prediction circuitry further comprises circuitry for updating said shift register by shifting in a preselected prediction value*. McFarling demonstrated that it was known at the time of invention to implement such history registers as shift registers and thus shift in a preselected prediction value (page 6, section 5, first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's history register as a shift register as found in McFarling's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated by the fact that such prediction schemes commonly use such history shift register configurations.

In regard to claim 39, Patt did not explicitly state *wherein the history register comprises a shift register*. McFarling demonstrated that it was known at the time of invention to implement such history registers as shift registers and thus shift in a preselected prediction value (page 6, section 5, first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's history register as a shift register as found in McFarling's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated by the fact that such prediction schemes commonly use such history shift register configurations.

In regard to claim 40, Patt did not explicitly state *wherein said method further comprises the steps of updating the shift register by shifting in a prediction bit*. McFarling demonstrated that it was known at the time of invention to implement such history registers as shift registers and thus shift in a preselected prediction value (page 6, section 5, first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's history register as a shift register as found in McFarling's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated by the fact that such prediction schemes commonly use such history shift register configurations.

7. Claims 27 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings

of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257, as applied to claims 23 and 35 above, respectively.

In regard to claim 27, Patt did not explicitly state the limitation *wherein said circuitry for updating said selector table is further operable to set a value in a selected entry in said selector table to a value associated with said fetch-based table when corresponding values from said bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome.* Patt did demonstrate that it was known at the time of invention to use two-level prediction, the fetch based table, for accuracy (page 255, section 4.1, first two sentences). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the selector table with setting a value to the fetch-based table as found in Patt's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to a have prediction selector, which increases its accuracy whenever possible.

In regard to claim 37, Patt disclosed the limitations:

i) *determining whether at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome* (page 252, section 3)

ii) *maintaining the current value of corresponding bits in the corresponding selector table entry when at the least one bit of both the first and second sets of*

branch prediction bits correctly predict the branch resolution outcome (page 252, section 3)

Patt did not explicitly state the limitation *updating the current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome*. Patt did demonstrate that it was known at the time of invention to use two-level prediction, the fetch based table, for accuracy (page 255, section 4.1, first two sentences). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the selector table with setting a value to the fetch-based table as found in Patt's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to a have prediction selector, which increases its accuracy whenever possible.

Remarks

8. The proposed drawing corrections submitted along with the amendment on 28 August 2002 are approved.

9. Examiner has considered Applicant's arguments with regard to claim 10 and found them to not be persuasive. Applicant argues that it would not have been obvious to replace Patt's two-bit counters with a one-bit counter. Applicant maintains Patt requires a two-bit counter in order to perform correctly. This of course is true if the invention had not been modified as indicated in the 103 rejection of the last office action. Examiner maintains this modification is obvious because: in order to pursue a simpler version of the invention one of ordinary skill in the art would have been

motivated to use a one-bit counter and thus not requiring the more accurate prediction mechanisms mentioned in the prior art. This could be for a variety of factors, such as less time for development or less chip space available.

10. Examiner further has considered Applicant's pseudo arguments with regard to new claims 21-40 and found them not persuasive. Furthermore the arguments, which simply state the cited prior art does not teach the limitations, do not meet for the minimum requirement for an argument. The arguments offer no support for their conclusionary statements. The above rejection is Examiner's argument.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
November 18, 2002

TUAN Q. DAM
PRIMARY EXAMINER